REMARKS

Final Rejection

The Examiner based the Final rejection status on an amendment by the Applicant. Specifically, the action was made final under MPEP §706.07(a) because "Applicant's amendment necessitated the new ground(s) of rejection." Applicant traverses the finality of the present office action. In response to the prior office action, Applicant merely corrected a typographical error in dependent claim 8.

Applicant's remarks were persuasive to remove the original rejection. The new rejection is based upon a new reference and the original claims. If the Examiner maintains that a New grounds of rejection was presented in the Final Action, Applicant believes that the Final Action is premature and should be withdrawn under MPEP 706.07(d).

In the Drawings

The proposed drawing corrections filed on April 1, 2002 were disapproved because they "introduced new matter into the drawings".

Applicant does not agree that removing surplus features from a figure constitutes new matter. Applicant has provided herewith a proposed drawing correction that merely removes the reference numbers for the protect circuit, low Vcc circuit and latch circuit. The features will remain in the Figure. Applicant notes that the vast majority of patent application and issued patents include features in the drawing that are not labeled with a reference number or detailed in the specification. As such, the proposed amendment does not constitute new mater and is appropriate.

Claim Rejections Under 35 U.S.C. § 112

Claims 1-27 were rejected under 35 U.S.C. § 112 as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the

claimed invention. The Examiner based the rejection upon the proposal of removing the surplus features of Figure 1. The Examiner further stated that Figure 15 was not described in the specification and that the latch circuit in claims 1-27 was not described.

Applicant respectfully traverses the rejection. The 35 U.S.C. § 112 rejection has been inappropriately applied. Clearly claims 1-27 contain subject matter that was described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Merely having, or removing, surplus features that were not recited in the claims cannot support a § 112 rejection.

Figure 15 is described in the specification at page 4, lines 23-24. A further description of the Figure is not required to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The write latches of claims 1-27 are clearly described on pages 41-43 of the specification and Figure 32.

Claims 16 and 25 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, that there was no antecedent basis for the "plurality of the plurality of memory blocks".

Claims 16 and 25 have been amended to correct this typographical error.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-27 were rejected under 35 U.S.C. § 102(b) as being anticipated by Baglee et al. (U. S. Patent No. 4,718,041). Applicant respectfully traverses the rejection.

The Examiner states that Figure 2 is a synchronous non-volatile memory citing column 3, lines 41-49 and column 11, lines 37-42. The Examiner further stated that the read cycle immediately followed a write cycle, citing lines 64-68 of column 1.

Applicant notes that timing circuit 42 of Figure 2 is an internal timing circuit for memory 28. As such, there are no external clock signals to constitute a synchronous memory as described in the present specification for zero bus latency turn around. In fact, the cited reference does not teach or describe clock cycles in the detailed description or drawings. Column 3, lines 41-49 and column 11, lines 37-42 of the reference describe the basic focus of the reference to extend the life of an EEPROM by performing an internal read operation following a write operation. The read operation is performed on the written data to verify the success of the write operation.

Claim 1 specifically recites that the write operation is executed on a first clock cycle and a read on the next clock cycle. Figure 4 of the reference appears to teach that a logical chain of events occurs to perform the read comparison operation. As such, there is no teaching of the specific timing of claim 1.

Claim 2 describes that the read and write operations are performed on different banks. The cited reference teaches a verification operation on the same memory cells. Therefore, there is not teaching of the different bank write/read operations.

Claims 3-5, 8 describe detailed operations that are not described in the cited reference.

Claim 6 recites that the data connections are released after latching write data. Further, claim 6 states that the read operation is performed while write data is transferred from write latches. The reference does not teach or suggest these claim limitations.

Claims 7, 9 and 11-13 clearly state that the read operation is initiated in response to an external read command. The cited reference fails to teach this limitation.

Claims 14-18 and 24-27 describe a memory with a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections. The cited reference fails to teach the write latch as claimed.

Claims 19-23 claim specific clock cycle timing not described in the cited reference.

Applicant maintains that the Examiner has failed to properly apply the reference to all of the limitations of all the claims. Specifically, there is no citation by the Examiner

indicating the timing features or latch structure claimed. The mere citation that an internal read verification is performed following a write operation does not anticipate claims 1-27.

CONCLUSION

Applicant believes that claims 1-27 are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions regarding this application, please contact attorney Russell D. Slifer at (612) 312-2202.

Respectfully submitted,

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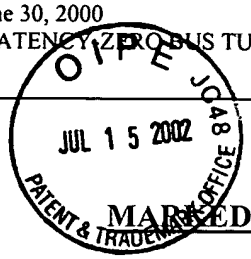

MARKED-UP VERSIONS OF AMMENDMENTS

IN THE CLAIMS

Please amend the following claims:

16. (Amended) The synchronous memory device of claim 15 wherein the memory array is arranged in a plurality of memory blocks, and the control circuitry is configured to copy the data from the write latch to a first block of the plurality [of the plurality] of memory blocks.

25. (Amended) The memory system of claim 24 wherein the memory array is arranged in a plurality of memory blocks, and the synchronous memory comprises control circuitry configured to copy the data from the write latch to a first block of the plurality [of the plurality] of memory blocks.